Amendments to the Drawings:

The attached sheets of drawings include changes to FIGs. 1-3. These sheets, which include FIGs. 1-4, replace the original sheets. FIGs. 1-3 have been changed to include the legend "Prior Art".

A marked-up version of the drawings, with revisions shown in red, is included with the amended drawings. Entry of the amended drawings is respectfully requested.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

Claims 1-10 are pending in the present application. Claims 1 and 6 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

The drawings are objected to for reasons indicated in the Office Action. The drawings are amended herein to add the legend "Prior Art" to Figures 1-3. It is believed that the objection to the drawings is overcome, and reconsideration thereof is requested.

Claims 1-4, 6-8 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Miller (U.S. Patent No. 4,959,557). Claims 5 and 9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Miller and Gutierrez (U.S. Patent No. 6,566,971). Reconsideration of the rejections and allowance the claims are respectfully requested.

The present invention as claimed in independent claim 1 is directed to a clock squarer. The clock squarer includes a semiconductor chip pad and an electrostatic protective circuit connected at a node, and a square wave generating circuit. The clock squarer further includes a capacitor provided between the node and the square wave generating circuit. A square wave having a stable duty is generated at an output of the square wave generating circuit in response to an input signal at the chip pad, irrespective of variance in environmental conditions. The capacitor prevents a leakage current from flowing between the square wave generating circuit and the electrostatic protective circuit.

The present invention as claimed in independent claim 6 is directed to a clock squarer. The clock squarer includes a semiconductor chip pad for connecting an external circuit with an internal circuit of a semiconductor chip. Further, the clock squarer includes an electrostatic protective circuit connected to the semiconductor chip pad at a node. A first terminal of a capacitor is connected to the node. A square wave generating circuit is connected to a second terminal of the capacitor for generating a square wave at an output terminal thereof based on an

input signal received at the semiconductor chip pad. The capacitor prevents a leakage current from flowing between the square wave generating circuit and the electrostatic protective circuit.

In the present invention as claimed in independent claims 1 and 6, a clock squarer circuit includes a "semiconductor chip pad", an "electrostatic protective circuit", a "capacitor", and a "square wave generating circuit". The "capacitor" is connected to a "node" which connects the "semiconductor chip pad" and the "electrostatic protective circuit". The "capacitor" reduces the "leakage current" flowing from the input terminal of the "square wave generating circuit" to the "electrostatic protective circuit". In this manner, the semiconductor chip pad and its associated electrostatic protective circuit are isolated from the square wave generating circuit by the capacitor, since the capacitor only allows high-frequency AC current to pass. Therefore, leakage current is prevented from flowing between the square wave generating circuit and the electrostatic protective circuit.

Neither APA nor Miller includes a "capacitor" that is "provided between" a "node" connecting a "semiconductor chip pad" and a "electrostatic protective circuit" and a "square wave generating circuit" as claimed in claim 1, or "having a first terminal connected to the node" and having a "second terminal" connected to "a square wave generating circuit"as claimed in claim 6. As stated in the Office Action, no such capacitor is present in the APA circuit.

Miller is cited in the Office Action as disclosing a capacitor connected between a crystal oscillator 40 (see Miller, FIG. 6) and a square wave generating circuit (the circuit between node 75 and resistor 51). In Miller, the capacitor 46 in conjunction with resistor 44, operates to remove the DC and low-frequency components of the AC signal generated by the crystal oscillator 40. No electrostatic protective circuit is present, and therefore leakage current is not of concern in the Miller system. For this reason, one would not have been motivated to apply the capacitor of Miller to the circuit of APA in order to reduce or prevent leakage current, since leakage current is not an issue in Miller and is therefore not mentioned in Miller. In any event, the combined teachings of APA and Miller fail to teach or suggest a "capacitor" provided

between a "node" connecting a "semiconductor chip pad" and a "electrostatic protective circuit" and a "square wave generating circuit", as claimed in claim 1, or "having a first terminal connected to the node" and having a "second terminal" connected to "a square wave generating circuit" as claimed in claim 6. Further, the combination of APA and Miller fails to teach or suggest a capacitor preventing "leakage current" from "flowing between the square wave generating circuit and the electrostatic protective circuit" as claimed in claim 1 and 6.

It is therefore submitted that independent claims 1 and 6 are in condition for allowance, and such allowance is respectfully requested. With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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Annotated Sheet Showing Changes

FIG. 1 (PRIOR ART)

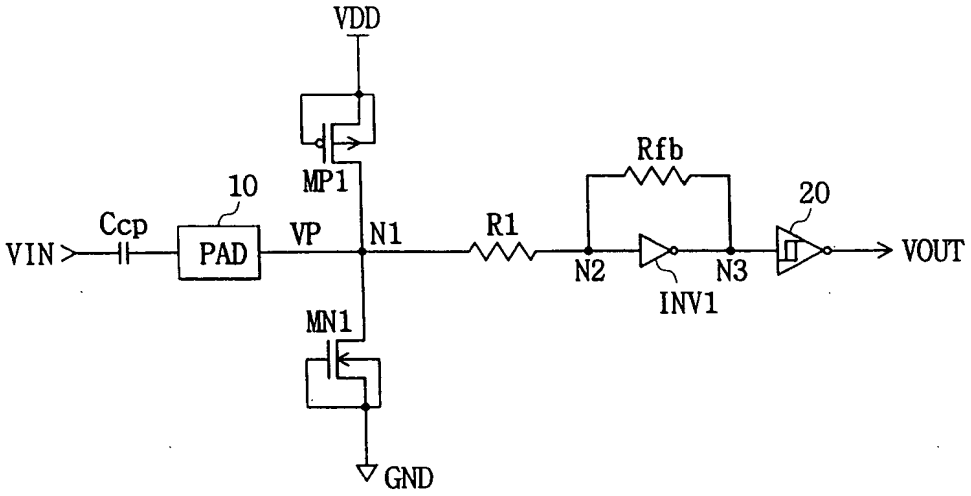

FIG. 2 (PRIOR ART)

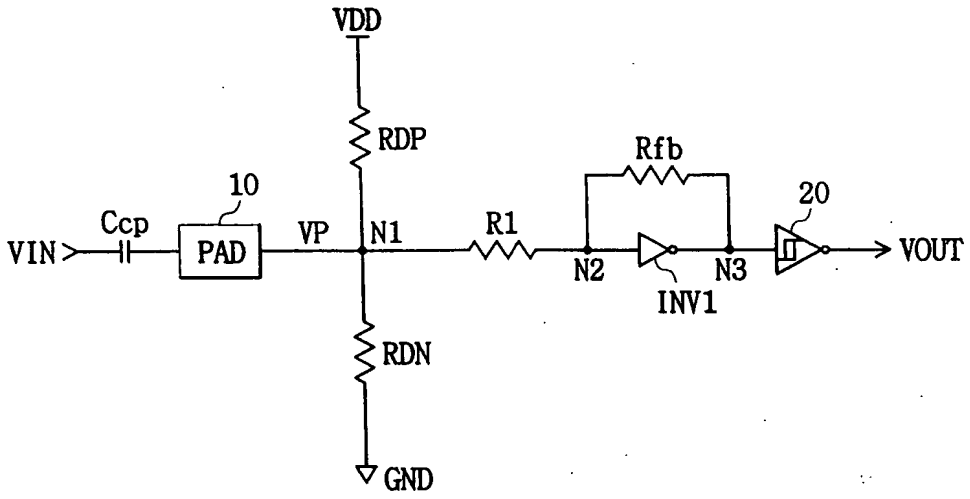

FIG. 3 (PRIOR ART)

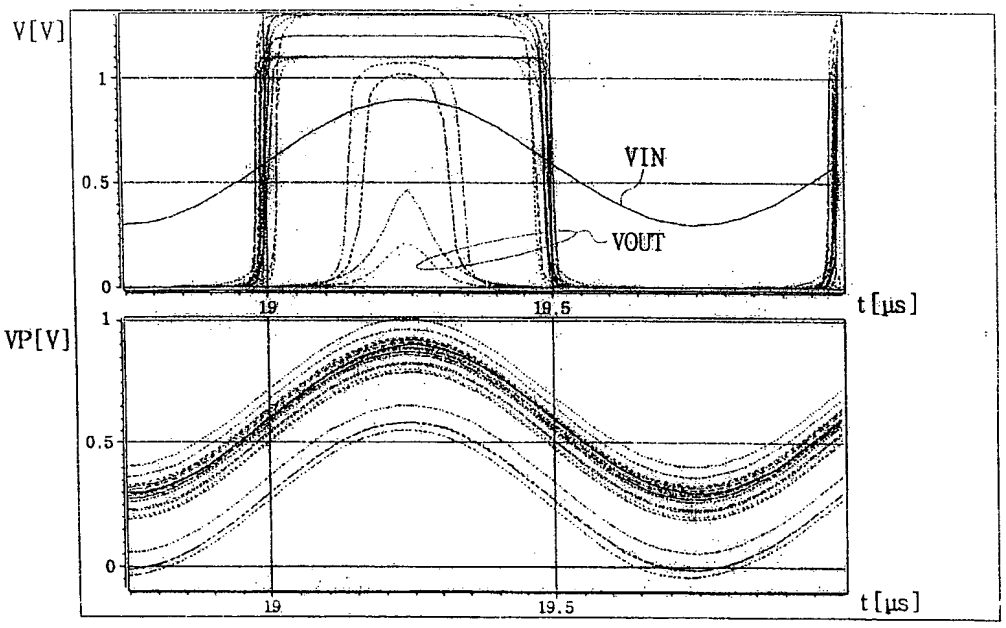

FIG. 4